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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,872	04/16/2004	Yee-Chia Yeo	N1085-00180 [TSMC2003-032	8595

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EXAMINER	
GHYKA, ALEXANDER G	

ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

(A)

Office Action Summary	Application No.	Applicant(s)	
	10/825,872	YEO ET AL.	
	Examiner	Art Unit	
	Alexander G. Ghyka	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *3,4,28 and 29* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-27,30 and 31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

ALEXANDER GHYKA
PRIMARY EXAMINER

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Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse in the reply filed on January 20, 2006 is acknowledged. The traversal is on the ground(s) that Figure 4 is not drawn to a gate electrode with a non-planar surface. This is not found persuasive because Figure 4 requires doping and annealing steps before planarizing the surface, whereas Figure 7, requires those steps after planarization of the gate electrode material.

The requirement is still deemed proper and is therefore made FINAL.

Applicants elect Species I which is drawn to Claims 1, 2, 4-27 and 30-31. The Examiner withdraws Claim 4, which is dependent on Claim 3 (Species II). Claims 1, 2, 5-27 and 30-31 are now under consideration.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 2, 5-7, 9-15, 18-27 and 30 are rejected under 35 U.S.C. 102 (a) or (e) as being anticipated by Mathew et al (US 2003/0151077).

The present Claims generally require a method of forming a gate electrode for a multiple gate transistor in a semiconductor device comprising providing a substructure comprising a semiconductor fin disposed over an insulating layer and a gate dielectric formed on said semiconductor fin; forming a gate electrode material over said gate dielectric and said semiconductor fin, said gate electrode having a top surface that is non-planar as formed; introducing dopant impurities into said gate electrode material; after said introducing, annealing to activate dopant impurities in said gate electrode; and planarizing said top surface to form a planarized top surface.

Mathews disclose a fin structure 24, overlying an insulating layer, and a gate dielectric 26 on the fin. See Figures 2-3 and paragraphs 17-19 on page 2. Mathews further disclose forming a gate electrode material 28 over said gate dielectric and said semiconductor fin, said gate electrode having a top surface that is non-planar as formed. See Figure 3 and paragraph 18, page 2. Moreover, Mathews et al disclose introducing dopant impurities into said gate electrode material; after said introducing, annealing to activate dopant impurities in said gate electrode. See Figures 5-7, paragraphs 20-21 of page 2, and the second sentence of paragraph 27 on page 3. Mathews also discloses planarizing said top surface to form a planarized top surface. See Figure 8 and paragraph 23 on page 2. Therefore Mathews anticipate Claims 1, 27 and 28.

With respect to Claim 2, Mathews disclose planarizing follows introducing and annealing. See Figures 5-7, paragraphs 20-21 of page 2, and the second sentence of paragraph 27 on page 3

With respect to claim 5, the gate electrode traverses the semiconductor fin. See Figures 8-9.

With respect to Claim 6, Mathews disclose source and drain regions as claimed. See Figure 8.

With respect to Claims 9-11, Mathews et al disclose spacers and patterning and implanting. See Figure 15, and page 2, paragraph 22.

With respect to Claims 12-15, Mathews et al disclose the semiconductor fin is formed of silicon and has a height greater than its width.

With respect to Claims 18-20, Mathews et al disclose a notch on the semiconductor film, and said gate electrode material filling the notch. See Figure 4.

With respect to Claims 21-26, Mathews et al disclose the gate electrode and gate dielectric materials as claimed. See paragraph 29 on page 2, and paragraphs 35-36 on page 4.

With respect to Claim 30, Mathews disclose the use of a masking layer to form source and drain regions. See paragraph 24, page 2.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 8, 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew et al (US 2003/0151077) in view of Dakshina-Murthy et al (US 6,803,631).

Mathew et al is relied upon as discussed above.

However, Mathew et al does not disclose performing selective epitaxy on exposed portions of the semiconductor film.

Dakshina-Murthy et al disclose the formation of a strained layer on a FinFet using selective epitaxial growth. See column 3, line 55 to column 4, line 10.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to perform selective epitaxial growth on exposed portions of the semiconductor fin in the process of Mathew et al, for its known benefit of forming a stained layer. As both references are drawn to Finfets, a *prima facie* case of obviousness is established.

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathew et al (US 2003/0151077) in view of Nowak et al (US 6,794,718).

Mathew et al is relied upon as discussed above.

However, Mathews et al do not disclose boron and phosphorus implantation at 1 X 10^{15} / cm^2 as required by the present claims.

Nowak disclose the formation of Finfet devices, and the implantation of boron and phosphorus. See column 5, lines 55-70.

It would have been obvious to one of ordinary skill in the art, at the time of the invention, to use boron and phosphorus implantation at 1 X 10^{15} / cm^2 in the process of Mathew et al, for their known benefit in the art as P type and N type dopants. The use of a known dopant, boron or phosphorus, for its known benefit, forming ource and drain regions, would be *prima facie* obvious to one of ordinary skill in the art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander G. Ghyka whose telephone number is (571) 272-1669. The examiner can normally be reached on Monday through Thursday during general business hours.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on (571) 272-1873. The fax phone

number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AGG
March 30, 2006

ALEXANDER GHYKA
PRIMARY EXAMINER

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